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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,848	06/26/2003	Brian Phelps	1823-US	5755

7590 01/23/2006

Teradyne, Inc.
Legal Department
321 Harrison Avenue
Boston, MA 02118

EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 01/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,848	PHELPS ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☒ Claim(s) *1;8 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 August 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-10 are presented for examination.

Drawings

Figures 2 and 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Oath/Declaration

The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because:

It does not identify the mailing address of each inventor. A mailing address is an address at which an inventor customarily receives his or her mail and may be either a home or business address. The mailing address should include the ZIP Code

designation. The mailing address may be provided in an application data sheet or a supplemental oath or declaration. See 37 CFR 1.63(c) and 37 CFR 1.76.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 3, 4, and 7 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. It is unclear to the examiner how "...wherein the generating test signals includes: creating a bus layout file" is accomplished or what generating bus layout files have to do with the generation of test signals. This is not enabled in the specification.

Claims 4 and 7 are dependent on claim 3 and therefore inherit the 35 U.S.C. 112, first paragraph issues of claim 3.

Claim 5 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. It is unclear to the examiner how "...wherein the step of generating test signals includes:

producing a list of packet and control entities" is accomplished through generating test signals with a semiconductor tester. This is not enabled in the specification.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Within the context of the above enablement issues, the limitations of claim 6 are not clearly defined.

Claims 3-7 will not be considered further on their merits until the enablement issues have been resolved.

Claim Objections

Claims 1, 8, and 10 are objected to for containing a plurality of elements or steps, which are not separated by a line indent. The following is a quotation of 37 CFR § 1.75(i):

(i.) Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation.

An amendment is required to put the claim in proper format. Line indents aid in understanding the logical grouping of a claim's elements.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 8 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Schinabeck et al. U.S. Patent No. 4,646,299.

As per claims 1, 8, and 10, Schinabeck et al. teach the claimed program on a readable medium, test system and method for testing semiconductor devices in which test signal applying and monitoring circuits are coupled to pins of an electronic device being tested to force test stimuli signals onto input pins of the device under test. The response signals are monitored while the device is being tested. Each test signal applying and monitoring circuit includes a node to be coupled to a pin of the device under test, a digitally programmed source for supplying a test signal connectable to the node by a first switch, and a comparison circuit connected to the node by a second switch for indicating the relative amplitude of the response signal with respect to a programmed reference level. The digitally programmed source is included for providing gated voltage-current crossover forcing functions during functional testing to minimize the disturbance when the device being tested is connected and to protect out of tolerance devices. Programmable voltage and current values define a pass window to assure a non-ambiguous go/no-go result during testing. (Abstract, column 4 line 56 through column 6 line 20, column 10 lines 19-34, column 21 lines 46-66)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 2, and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miura U.S. Patent No. 6,789,224 in view of Rivoir U.S. Publication No. 2002/0188888 A1

As per claims 1, 8, and 10 Miura et al. teach the claimed software, system and method for testing semiconductor devices, including generating test signals, applying the generated test signals to the device-under-test, capturing actual output entities from the DUT in response to the applied generated test signals comparing the actual output entities to expected output entities and identifying a fail condition where a comparison fails to match an actual output entity to an expected output entity (column 1 lines 22-44, Figure 1). Not explicitly disclosed is that if a failure is identified in the comparing step, defining a window of valid expected entities and comparing the failed actual output entity to the window of valid expected entities.

However, in an analogous art, Rivoir discloses a circuit in which a window of valid expected values are used to determine f a circuit fails or passes a test (Abstract, Figures 2 and 3). Therefore, it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the "window of valid expected entities". This would have been obvious as in any typical test design there are what is known in the art as "don't care" values (1's or 0's which are at times masked out of the test results) and this would define a window of valid test results or expected entities.

As per claims 2 and 9, Rivoir teaches (Figure 3C elements 124c-e) the claimed further comparing the failed actual output entity to the window of valid expected entities leads to a match between the failed actual output entity and any one of the valid expected entities in the window.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

"TRIM: Testability Range by Ignoring the Memory" by Carter et al. in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* Publication Date: Jan 1988 Volume: 7, Issue: 1 page 38-49 INSPEC Accession Number: 3130635

The testability by random test patterns of faults in the logic surrounding embedded RAMs is studied. Upper and lower bounds on the probability that a fault is caught are obtained by analyzing a modified, purely combinational circuit without the RAM. This analysis can be done with standard testability analysis techniques. The analysis is applied to an embedded two-port RAM.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
Examiner
Art Unit 2138